1. A method comprising:

receiving a processor identifier;

receiving a seed stored in a non-volatile memory; and

hashing said identifier and said seed to develop a device key.

2. The method of claim 1 further including requesting a random number and hashing said identifier and said seed with said random number.

3. The method of claim 2 including causing a processor to execute instructions to obtain a processor serial number.

4. The method of claim 1 including obtaining said processor identifier by executing instructions at the operating system kernel level.

5. The method of claim 2 including causing a processor to obtain a random number from an integrated circuit and generating a certificate.

6. The method of claim 5 including causing the processor to send said certificate to said integrated circuit.

7. The method of claim including causing said integrated circuit to validate said certificate and process said certificate to generate a device key.

8. The method of claim 7 including encrypting a new device key using a current device key and writing the encrypted new device key back to the processor.

9. The method of claim 7 including writing said device key into a memory in said integrated circuit.

10. The method of claim 1 including receiving a digital television broadcast from a head end and sending said device key to said head end.

11. An article comprising a medium storing instructions that enable a processor-based system to:

receive a processor identifier;

receive a seed stored in a non-volatile memory; and

hash said identifier and said seed to develop a device key.

12. The article of claim 11 further storing instructions that enable the processor-based system to

request a random number and hash said identifier and said seed with said random number.

13. The article of claim 12 further storing instructions that enable the processor-based system to execute instructions to obtain a processor serial number.

14. The article of claim 11 further storing instructions that enable the processor-based system to obtain said processor identifier by executing instructions at ring 0.

15. The article of claim 12 further storing instructions that enable the processor to obtain a random number from an integrated circuit and generate a certificate.

16. The article of claim 15 further storing instructions that enable the processor-based system to send said certificate to said integrated circuit.

17. The article of claim 16 further storing instructions that enable the processor-based system to cause said integrated circuit to validate said certificate and process said certificate to generate a device key.

18. The article of claim 17 further storing instructions that enable the processor-based system to encrypt a new device key using a current device key.

19. The article of claim 17 further storing instructions that enable the processor-based system to write said device key into a memory in said integrated circuit.

20. The article of claim 11 further storing instructions that enable the processor-based system to receive a digital television broadcast from the head end and send said device key to said head end.

21. An integrated circuit comprising:

an interface to couple said circuit to a processor-based system;

a transport demultiplexer coupled to said interface to receive audio/video content information;

a key logic circuit to extract a device key from a bit stream including a processor serial number and a device key seed; and

a memory to store said device key.

22. The circuit of claim 21 wherein said memory is part of said transport demultiplexer.

23. The circuit of claim 21 including a bus that couples said interface, said transport demultiplexer and said key logic circuit.

24. The circuit of claim 21 wherein said key logic circuit generates a random challenge on request from said processor-based system.

25. The circuit of claim 21 wherein said key logic circuit receives a certificate from said processor-based system and processes said certificate to generate a device key.

26. The circuit of claim 25 wherein said key logic encrypts a new device key using a current device key.

27. A processor-based system comprising:

a processor that stores instructions that enable said processor to obtain a processor serial number;

a non-volatile memory, coupled to said processor, to store a device key seed;

an integrated circuit coupled to said processor, said integrated circuit including a key logic circuit that generates a random challenge upon request from said processor.

28. The system of claim 27 wherein said key logic circuit extracts the device key from a bit stream including a processor serial number and a device key seed.

29. The system of claim 28 including a memory in said integrated circuit, said key logic circuit enabling said device key to be stored in said memory.

30. The system of claim 29 wherein said integrated circuit includes a transport demultiplexer that receives content from an external source, said memory being included as part of said transport demultiplexer.